REMARKS

Claims 1-41 are now presented for examination. Claims 2, 6, 9, 10, 12 and 13 have been cancelled without prejudice or disclaimer of subject matter. Claims 1, 11 and 19 have been amended to define still more clearly what Applicant regards as his invention, in terms which distinguish over the art of record. Claims 20-41 have been added to assure Applicant of the full measure of protection to which he deems himself entitled. Claims 1, 11 and 31 are the only independent claims.

The drawings have been objected to in that no "1006" appears in Fig. 7, "200A" appears in Fig. 1 while the specification at line 4 of page 8 refers to "200" and stippling is used in Figs. 1-3, 5-8, 9B and 14-16. It is proposed that Fig. 1 be changed to place the A used to depict sectioning below "200", to insert 1006 in Fig. 7 to replace the "1200" as indicated and to replace the stippling in Figs. 1-3, 5-8, 9B and 14-16 with diagonal hatching. The proposed changes are shown indicated in red in the enclosed drawing sheets. Approval of the changes is respectfully requested.

The specification and the abstract have been carefully reviewed and amended as to matters of form. With respect to the Examiner's objections, the specification has been amended at line 9 of page 1 to correct the spelling of "gate", at line 9 of page 12 to correct the typographical

error in "the" and at line 23 of page 24 to correctly denote "MOSFET". In addition, further changes have been made to improve idiomatic English. For example, "for enabling stable mass production and the characteristics of the SOI device are still retained" has been changed to "to enable stable production while retaining the characteristics of the SOI device".

Claim 11 has been objected to as being dependent upon a rejected base claim but has been indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 11 has been rewritten to incorporate all of the limitations of base Claim 1 and intervening Claim 9 and is believed to be allowable. Newly added Claims 21-30 depend from Claim 11 and recite further features of the invention of Claim 11 as amended which are shown in the drawings and disclosed in the specification. No new matter is believed to have been added. In view of the allowability of Claim 11 as amended, newly added Claims 21-30 are believed to be allowable.

Claims 1, 3, 14 and 19 have been rejected under 35 U.S.C. § 102(b) as anticipated by Kawabuchi. Claims 4 and 15-18 have been rejected under 35 U.S.C. § 103 as unpatentable over Kawabuchi. Claims 5-8 have been rejected as unpatentable over Kawabuchi in view of Yazawa et al. With

regard to the claims as amended, these rejections are respectfully traversed.

Claim 1 as amended is directed to a semiconductor device having first conductive type source and drain regions, a semiconductor layer including a channel region between the source and drain regions, an insulating layer covering at least the channel region and a gate electrode close to the insulating region. The channel region includes a first channel area of second conductivity type and of low resistivity close to the insulating region, a second channel area of the first conductivity type and of high resistivity close to the first channel area and a third channel area close to an additional insulating layer. An electrically neutral area is formed in the third channel area at a side adjacent to the additional insulating area.

In Applicant's view, Kawabuchi discloses a semiconductor device in which breakdown voltage and reduced injection of hot carriers are improved by providing reverse conductive type layers to the source and drain on the surface layer of a channel forming region and providing the same conductive type layer at an impurity density lower than the source and drain between the layer and a substrate.

As is well known, making the semiconductor layer thickness very thin depletes the channel and reduces coarse interface, horizontal electric field and ion scattering. It is, however, very difficult to make a very thin but stable

channel layer that can reduce the adverse effect of surface coarseness. The problems of a very thin channel layer are solved according to the present invention by providing a third channel area in addition to a pair of opposite conductivity channel areas which third channel area includes an electrically neutral area. As a result of the third channel with the neutral area feature, the prior art problems of a very thin channel are solved in a novel manner.

It is a feature of Claim 1 as amended that a channel region includes a third channel in addition to a one conductivity type low resistivity first channel area close to an insulating layer and an opposite conductivity type high resistivity second channel area close to the first channel area. The third channel area is close to an additional insulating layer and an electrically neutral area is formed in the third channel area at a side adjacent to the additional insulating area. Advantageously, according to the present invention, the layer thickness and impurity concentration are selected to make a portion of the third channel area into a neutral area. Kawabuchi may show a channel region divided into channel areas. The Kawabuchi arrangement, however, is devoid of any disclosure or teaching of the formation of a neutral area in a third channel area as in Claim 1.

Further, when a semiconductor region formed on an insulating substrate is depleted in an area in the vicinity

of the interface between the semiconductor and the insulating substrate, it is a problem that a channel is formed and leakage current flows between source and drain due to a surface state at the interface. As recognized by the Examiner, Kawabuchi does not disclose a structure with an insulating substrate and therefore does not in any manner consider the third channel area with the neutral area portion features of Claim 1. In at least these respects, Claim 1 as amended is believed to be completely distinguished from Kawabuchi and allowable.

Newly added Claim 31 is directed o a semiconductor device with source and drain regions of a first conductivity type and high impurity concentration, a semiconductor layer including a channel region between the source and drain regions, an insulating layer at least on the semiconductor layer and a gate electrode on the insulating layer. The semiconductor layer includes a first area of low resistivity and second conductivity type opposite the first conductivity type adjacent to the insulating layer, a fourth area of first conductivity type adjacent to the first area, a second area of the first conductivity type adjacent to the fourth area and a third channel area of the second conductivity type adjacent to the second area.

The features of Claim 31 and Claims 32-41 depending therefrom are shown in at least Fig. 15 of the drawings and

are described in the corresponding portions of the specification. No new matter is believed to have been added.

It is a feature of newly added Claim 31 that a semiconductor layer includes a first area of low resistivity and second conductivity type opposite the first conductivity type adjacent to the insulating layer, a fourth area of first conductivity type adjacent to the first area, a second area of the first conductivity type adjacent to the fourth area and a third channel area of the second conductivity type adjacent to the second area. While Kawabuchi may show a channel region with plural areas, the structure of the plural areas of Kawabuchi is completely different from that of Claim 31.

In particular, Kawabuchi is devoid of a third channel area of conductivity type opposite to that of the source and drain regions as in Claim 31. Further, while the Kawabuchi structure may has a layer of opposite conductivity type to that of source and drain adjacent to the insulating layer as in Claim 31, the next two layers (Kawabuchi Fig. 4d) are of opposite conductivity types. In Claim 31 the fourth and second areas are of the same conductivity type. It is therefore believed that newly added Claim 31 is completely distinguished from Kawabuchi and is allowable thereover.

In Applicant's opinion, Yazawa et al. discloses a MOSFET provided with a gate insulating film formed on a semiconductor surface between source and drain regions. A

gate electrode is formed on the gate insulating layer and a channel region sandwiched between the source and drain regions has a first layer and a second layer. The first layer lies beneath the gate insulating film and is opposite in conductivity type to the source and drain regions. The second layer lies beneath the first layer and has the same conductivity type as the source and drain regions. The length of the second layer between source and drain regions is greater than the length of the first layer between source and drain regions.

As discussed with respect to Kawabuchi, Yazawa et al. requires a channel region of a completely different structure than that of Claim 31. In Yazawa et al., the channel region of Figs. 6A and 18 have only two channel areas of different geometry than that of Claim 31. Further, Yazawa et al. is devoid of a third channel area as in Claim 31 and operates is a completely different way. Accordingly, it is believed that newly added Claim 31 is completely distinguished from Yazawa et al. and allowable thereover.

Neither Kawabuchi nor Yazawa et al. in any manner teach or suggest the channel region structure of Claim 31 that features four areas as in Claim 31. As a result, it is not seen that any combination of Kawabuchi et al. and Yazawa et al. in any manner suggests the channel region structure or operation of Claim 31. It is therefore believed that newly

added Claim 31 is completely distinguished from Kawabuchi and Yazawa et al. taken alone or in combination and is allowable.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable consideration and reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 758-2400. All

correspondence should continue to be directed to our below listed address.

Respectfully submitted,

Attorney for Applicant

Registration No. 24,225

FITZPATRICK, CELLA, HARPER & SCINTO
277 Park Avenue
New York, New York 10172
Facsimile: (212) 758-2982
F502\A141505\md